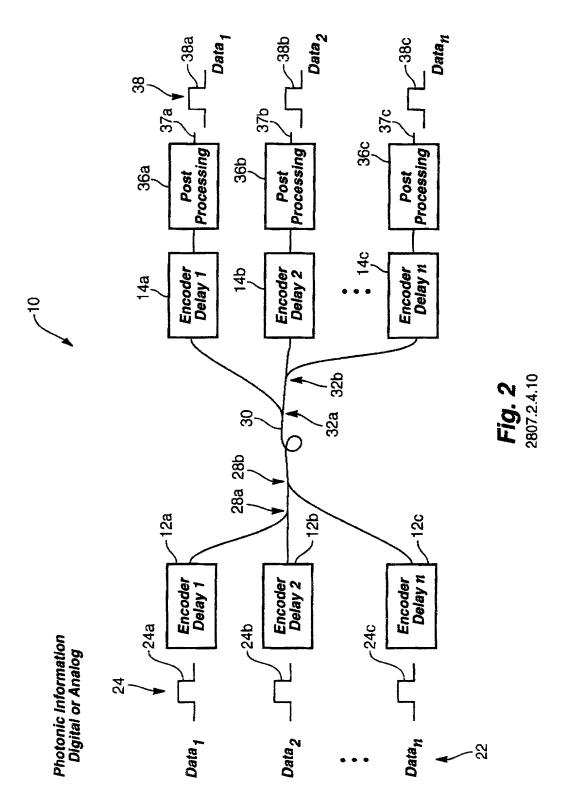
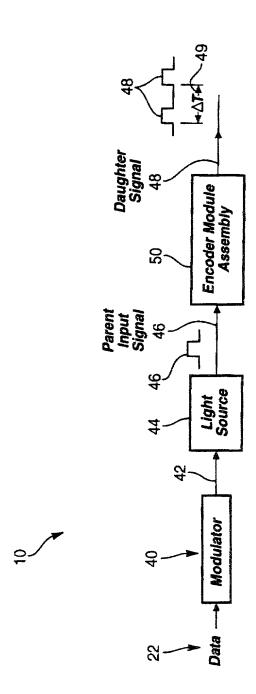


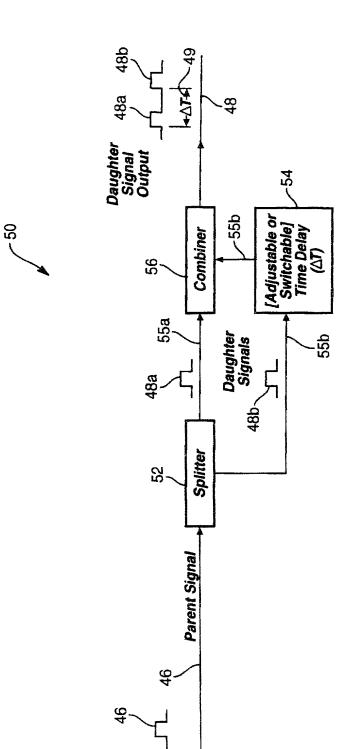
FIG. 1 2807.2.4.10





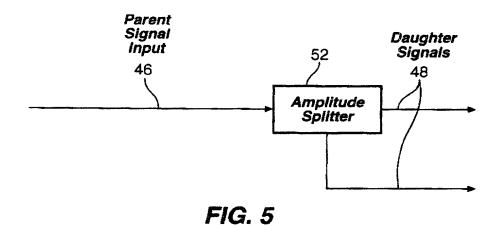
Differential Delay Multiplexer Sender/Encoder

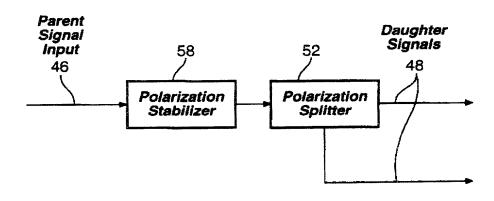
Fig. 3 2807.2.4.10



Differential Delay Multiplexer (DDM) Sender/Encoder

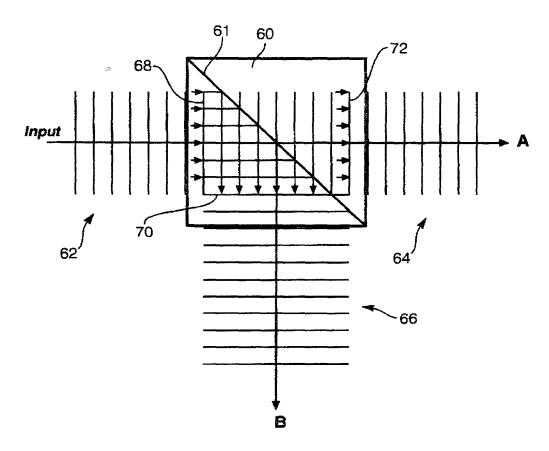
Fig. 4 2807.2.4.





Splitting Criteria

FIG. 6 2807.2.4.



Amplitude or Polarization Splitter

FIG. 7 2807.2.4.

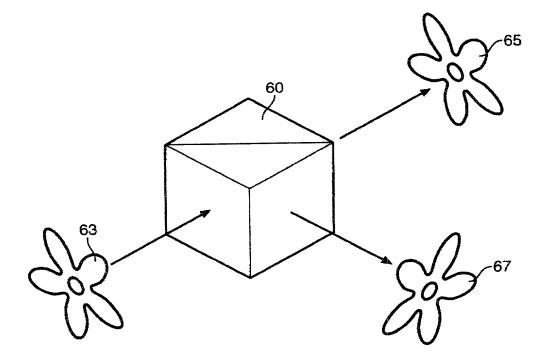
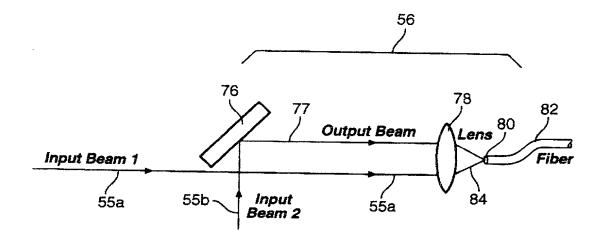


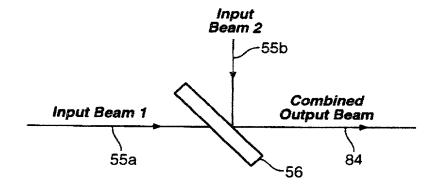
Image Signals Which Maintain Spatial Information

FIG. 7A

2807.2.4.



Beam Combiner FIG. 8



Amplitude or Polarization Combiner

FIG. 9

2807.2.4.

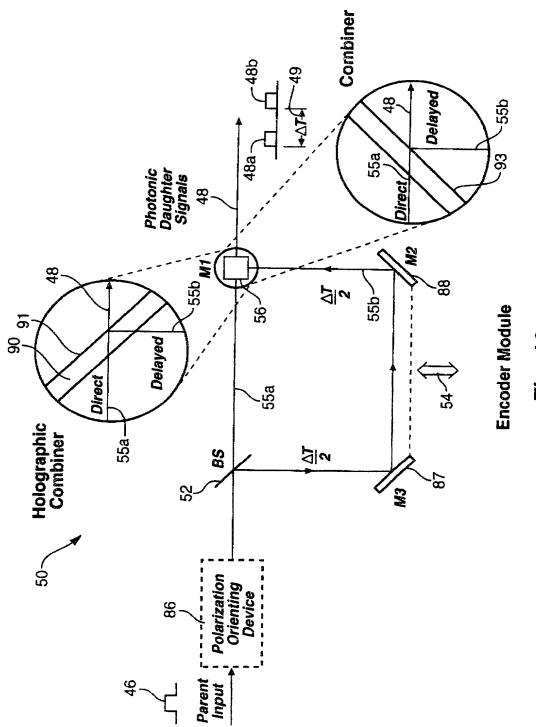
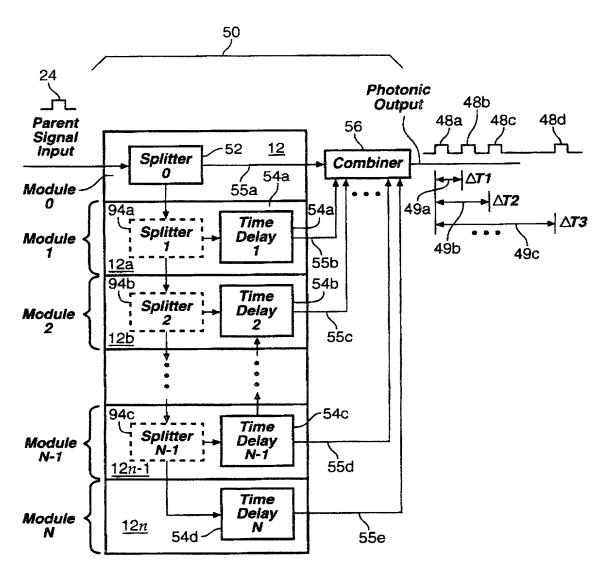


Fig. 10 2807.2.4.



Composite Encoder Module Assembly

FIG. 11 2807.2.4.

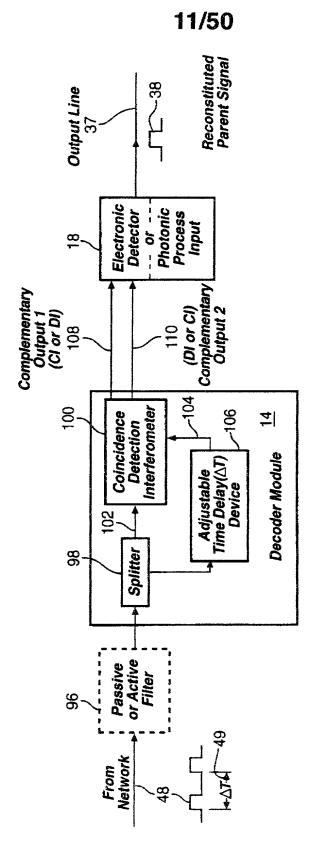


Fig. 12

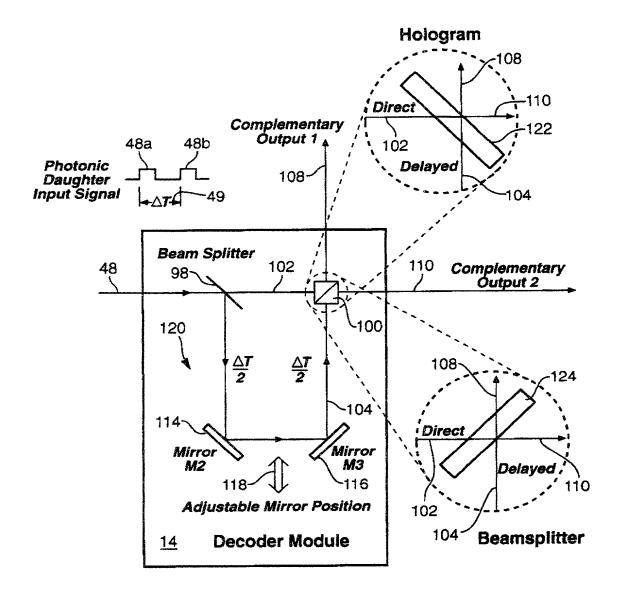


FIG. 13

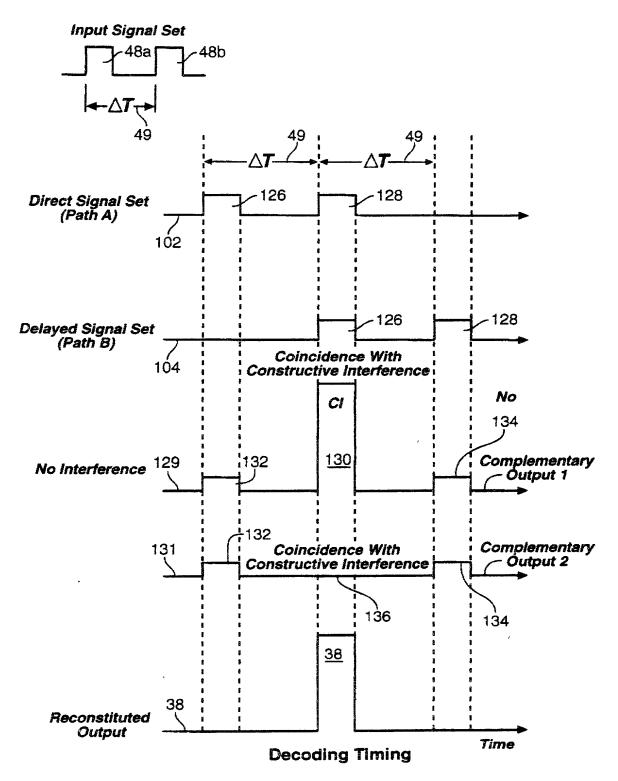


FIG. 14



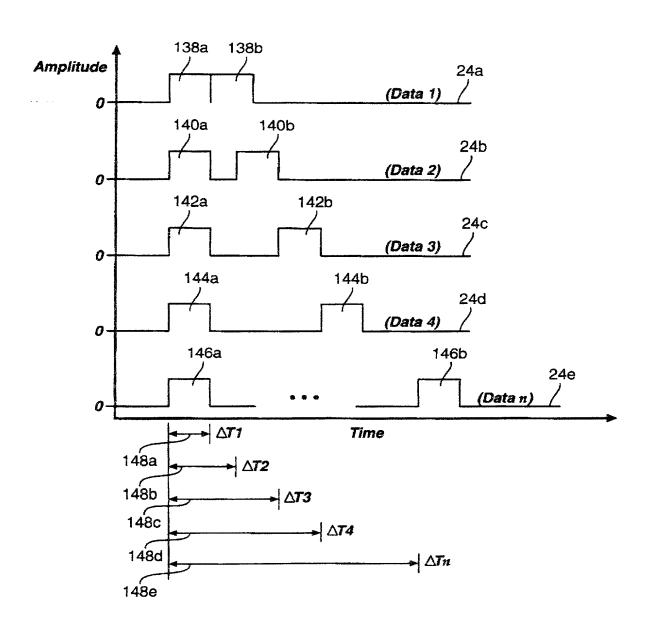


Fig. 15

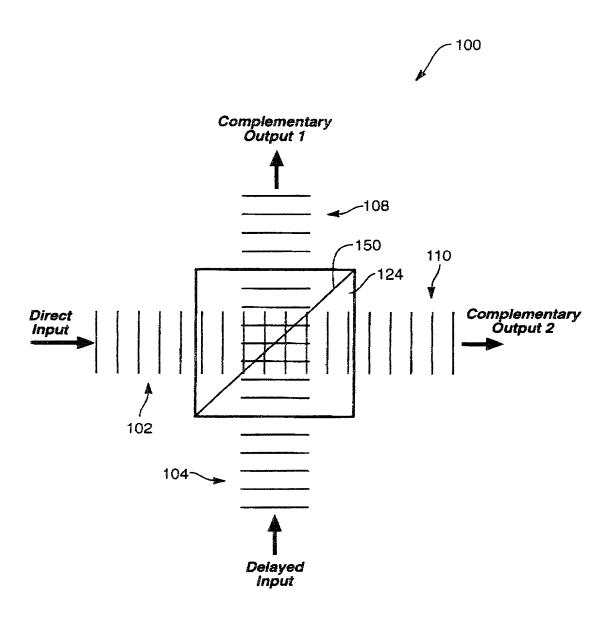


Fig. 16

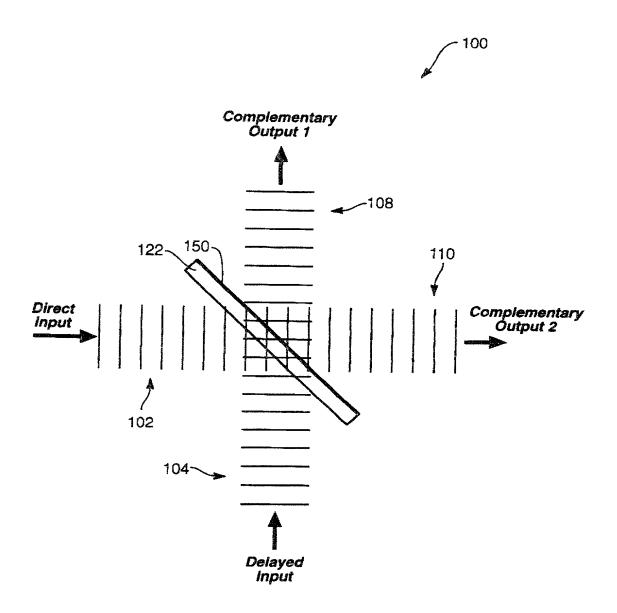


Fig. 17

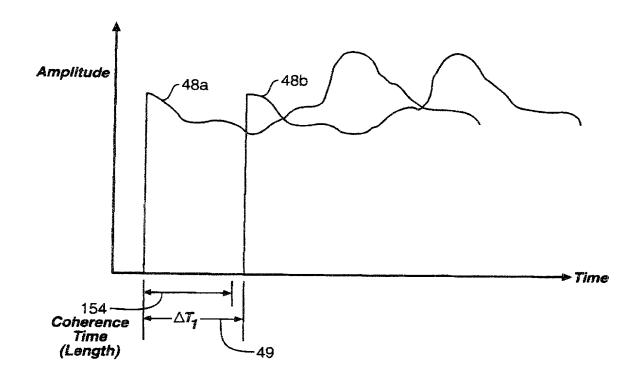


Fig. 18

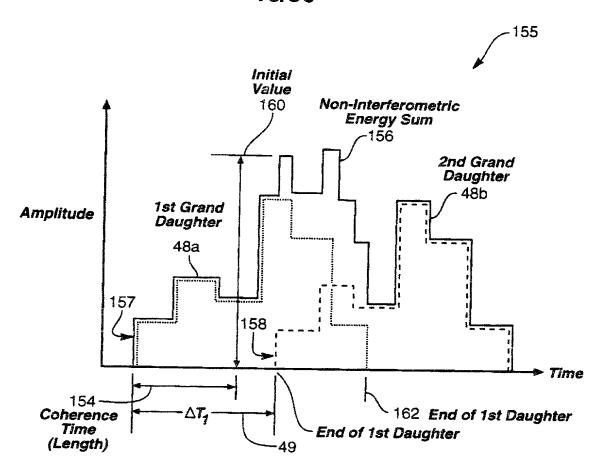


Fig. 19

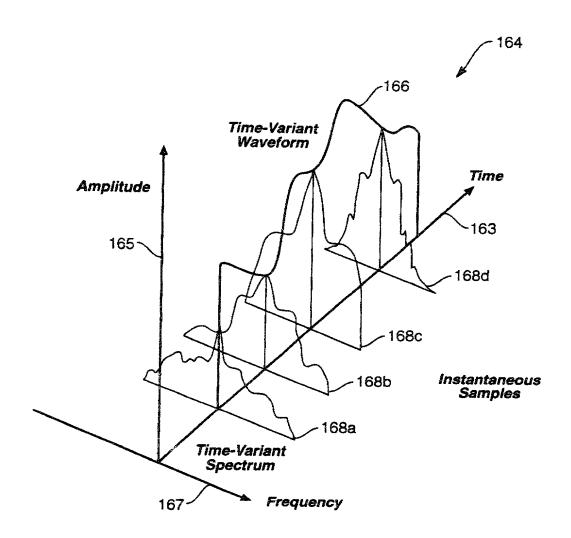
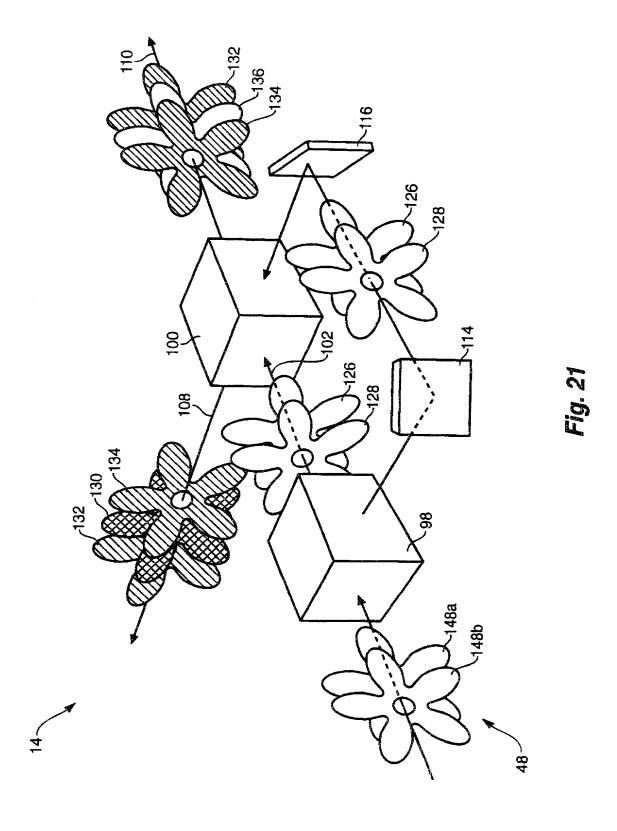
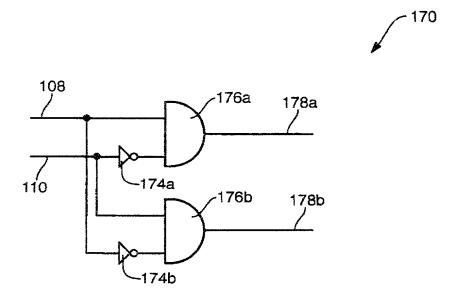
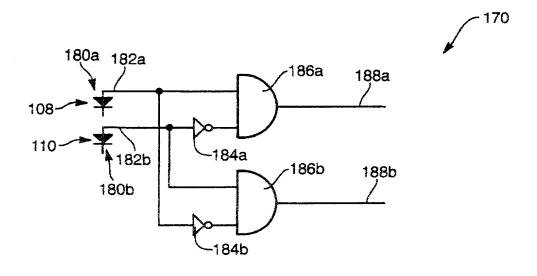


Fig. 20



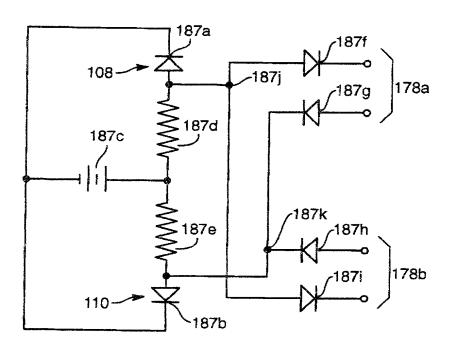


Photonic Processor Fig. 22



Electronic Processor Fig. 23A

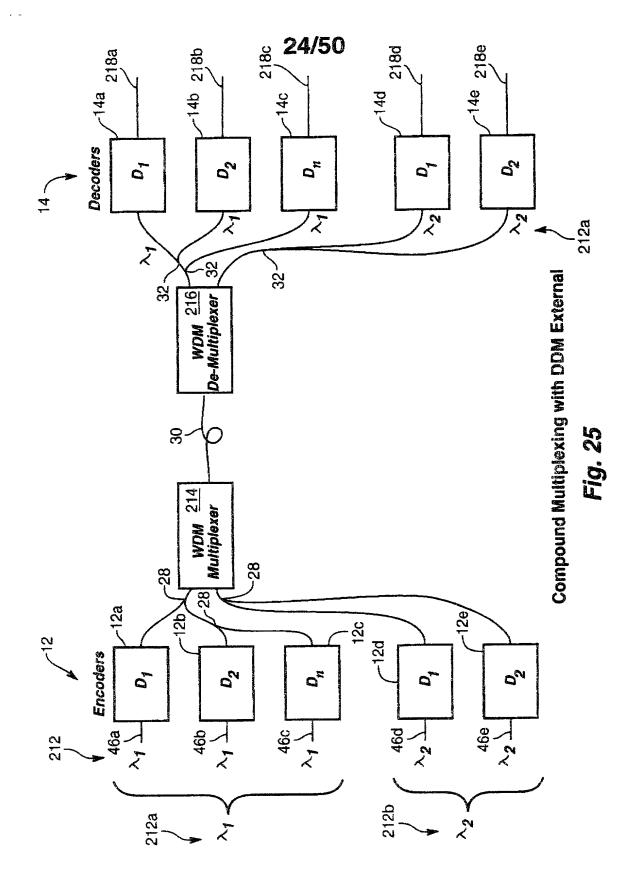


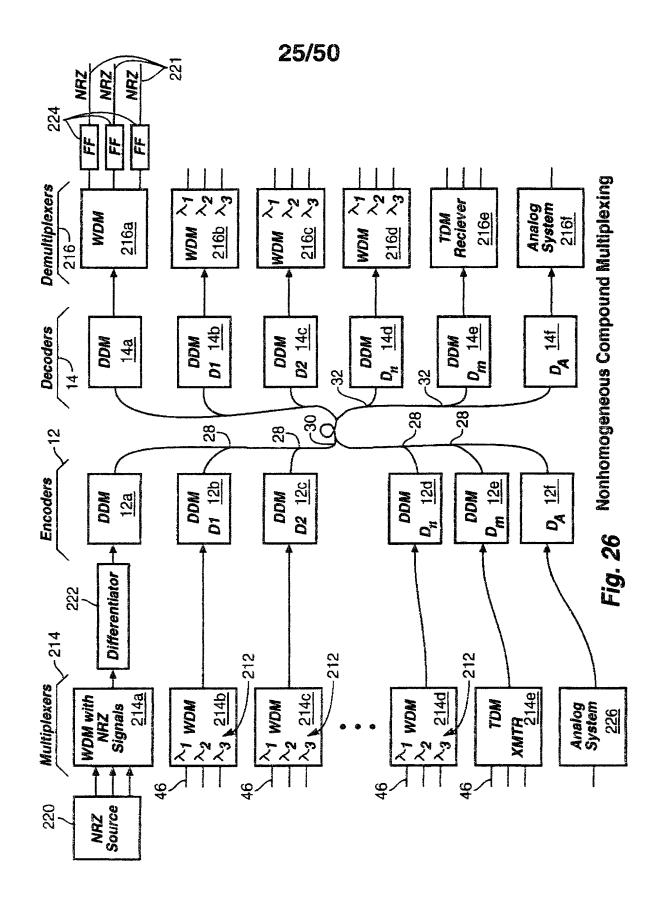


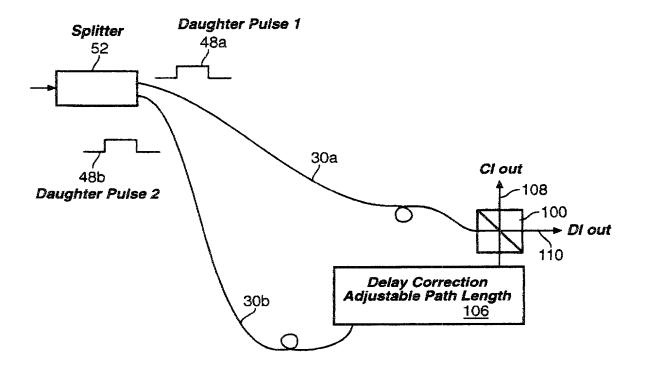
Electronic Processor

Fig. 23B

Fig. 24





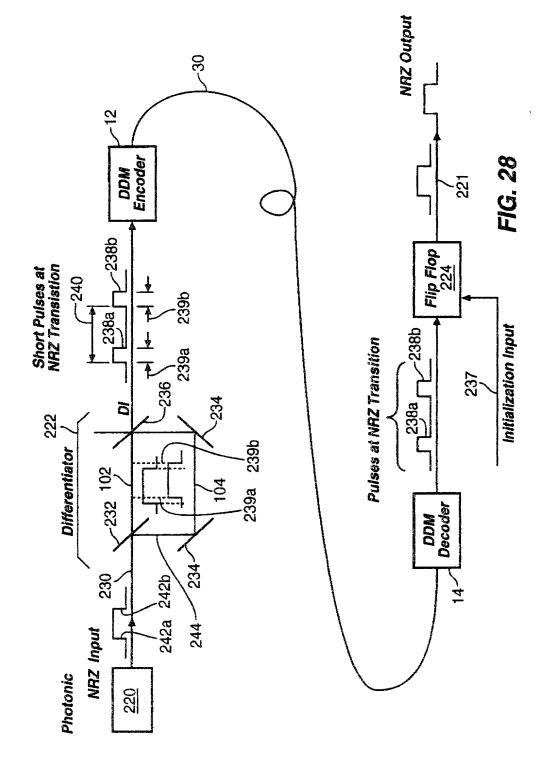


Multiple Delay Path

Integrated Delay and Delay Correction

FIG. 27

Photonic NRZ Interface



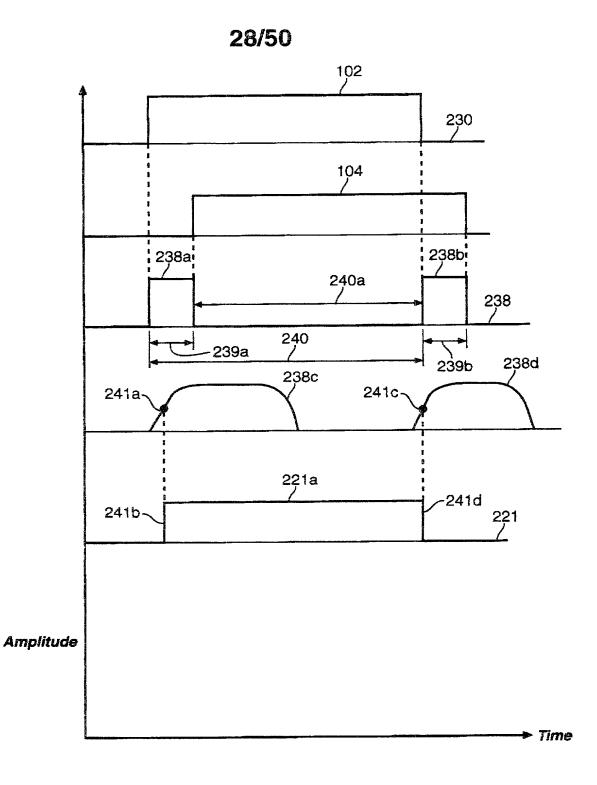
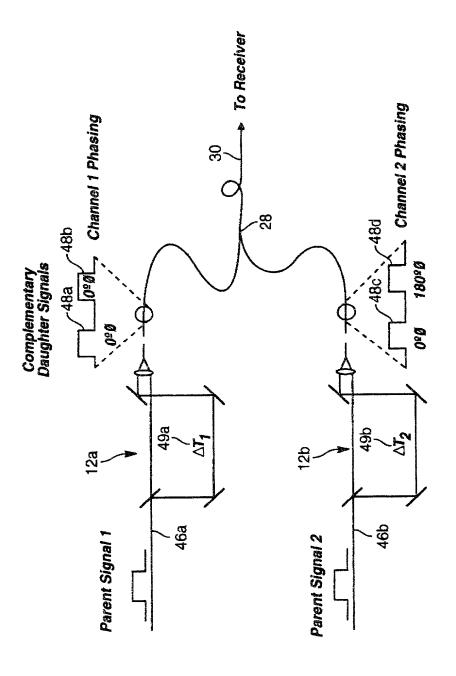


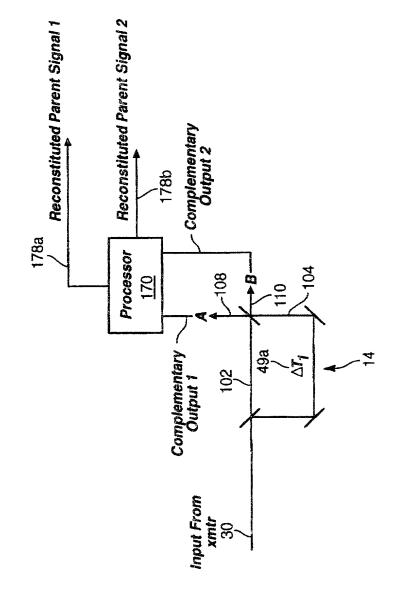
FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

Phase Sequenced Dual Channel Decoder



Phase Sequence Timing

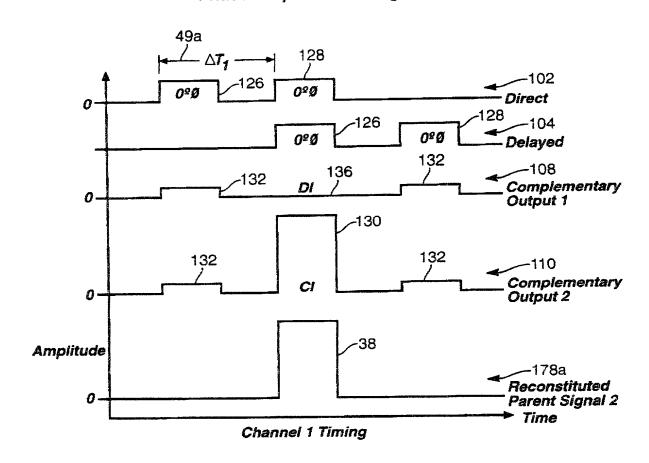


FIG. 32

Phase Sequence Timing

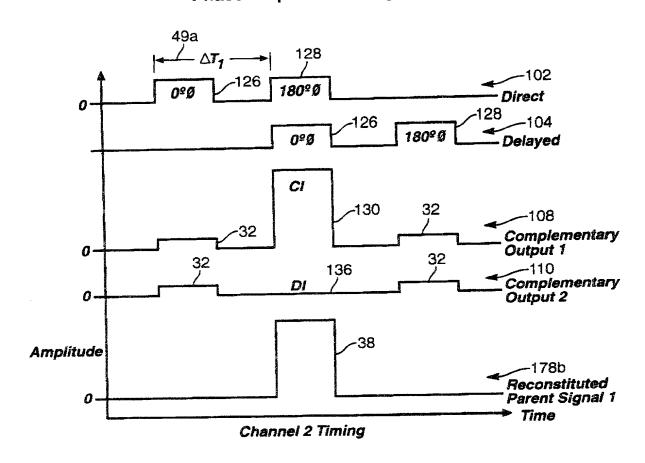
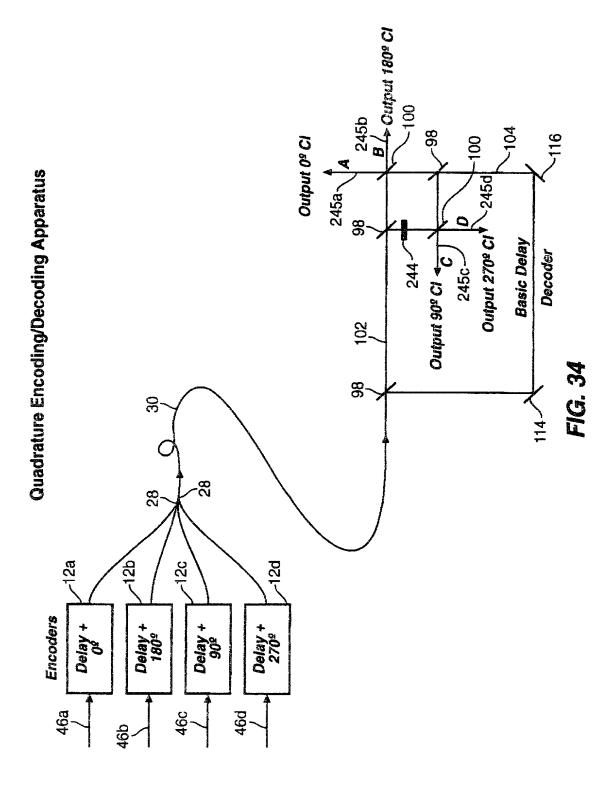


FIG. 33



	Phase of	Phase of Delayed Signal	Quadrature Outputs		
46a	Direct Signal		A	8	C D
Channel 1	0	o	CI	DI	C = D
Channel 2	o	180	DI	CI	C = D
Channel 3	0	90	A =	B	CI DI
Channel 4	0	270	A =	8	DI CI
			*	4	* *
			245a	245b	245c 245d

FIG. 35

35/50

Quadrature Wave Forms For One Channel

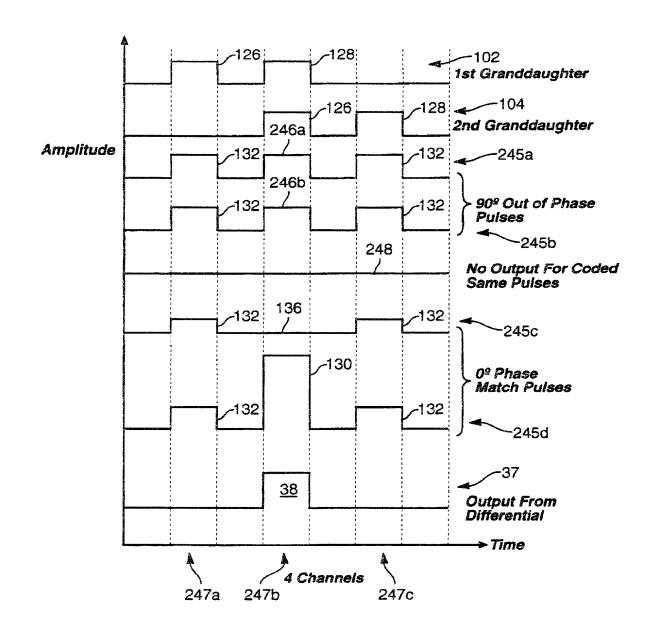


FIG. 36

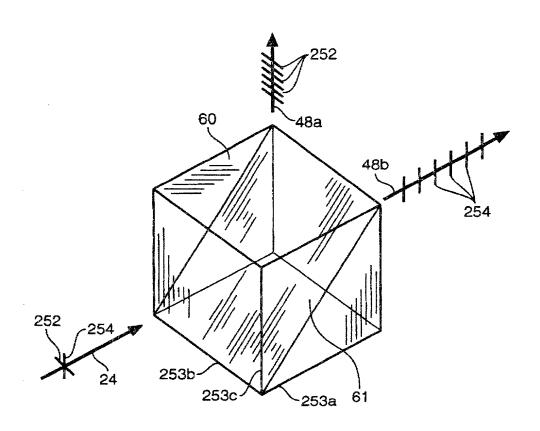


FIG. 37A

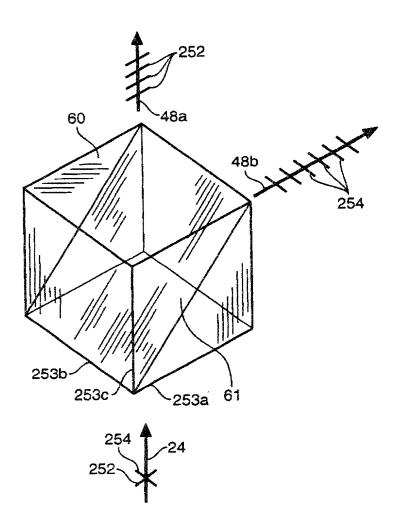
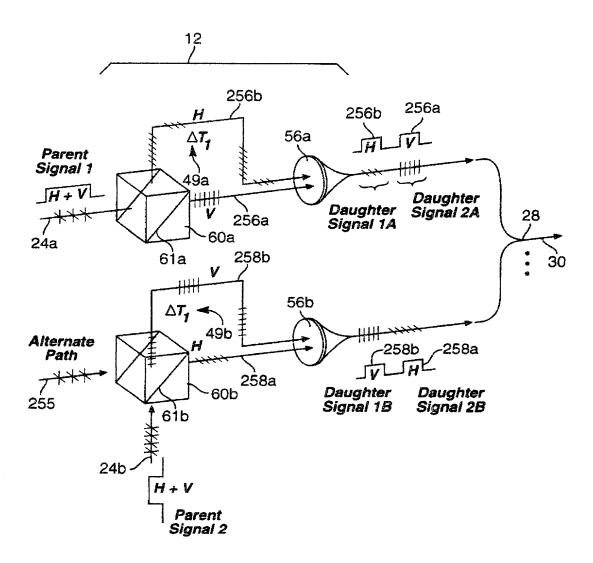
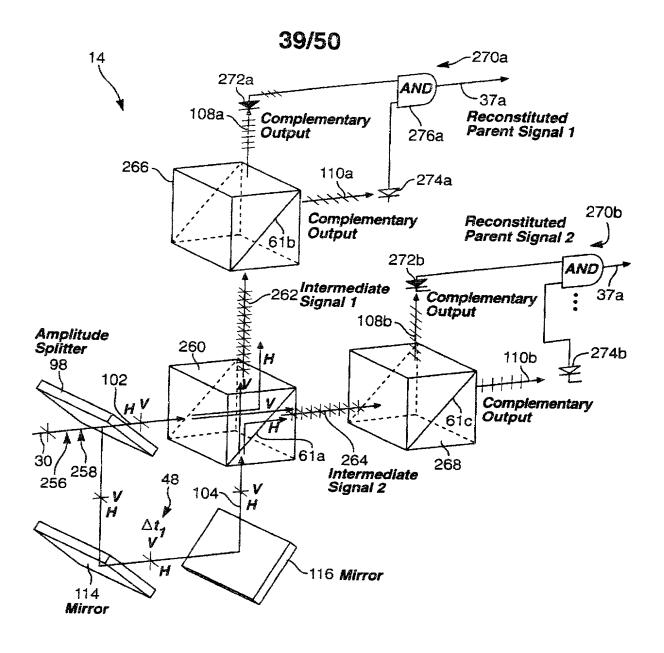


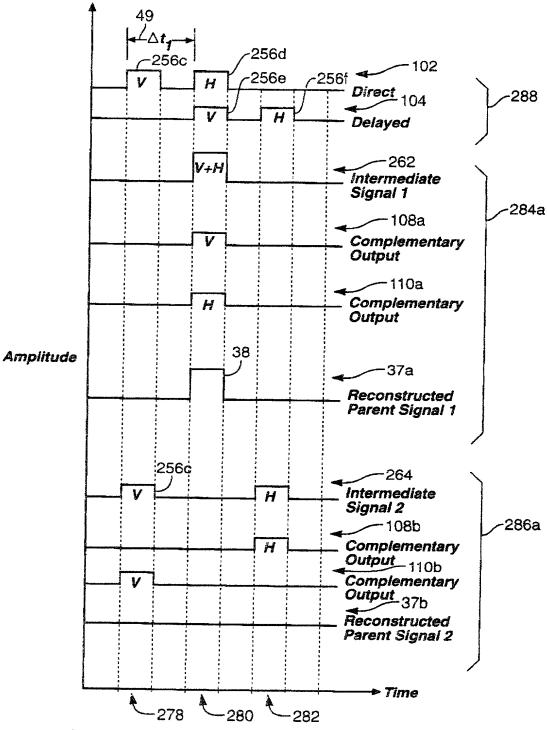
FIG. 37B



Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Double Decoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Polarization Sequenced Channel 1 Timing FIG. 40

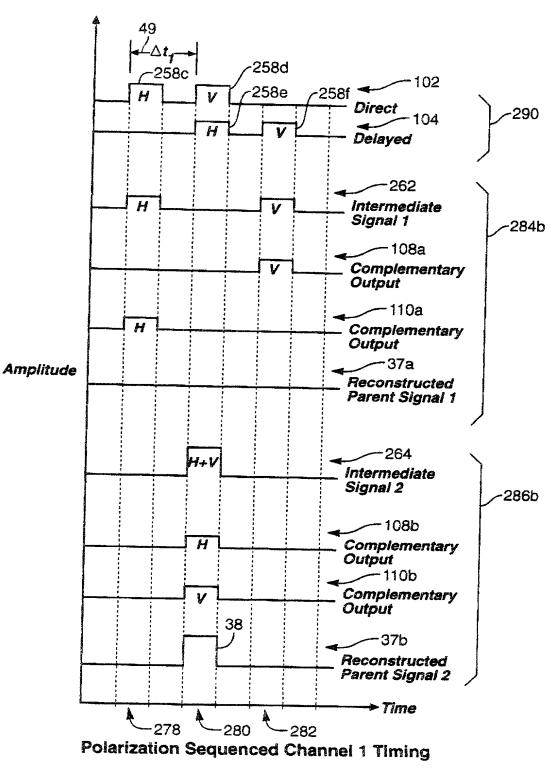


FIG. 41



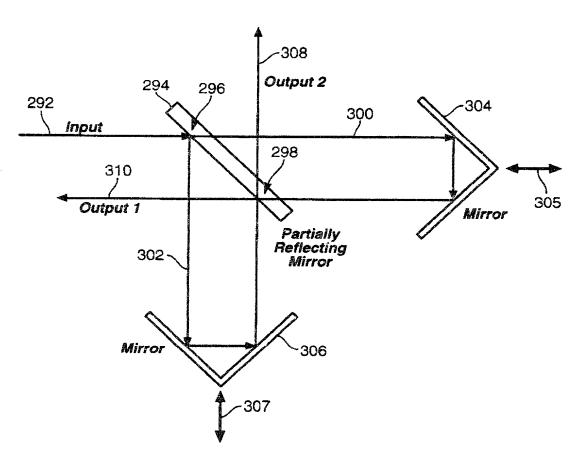
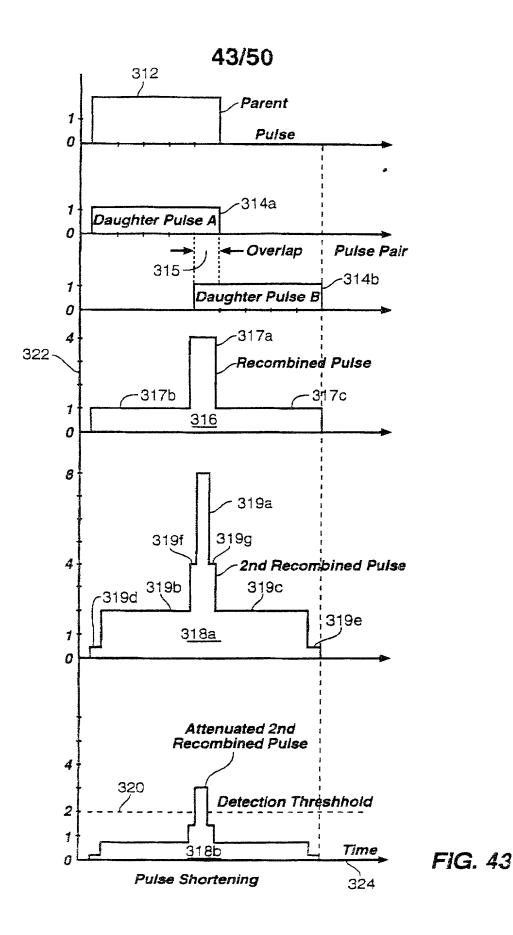


FIG. 42



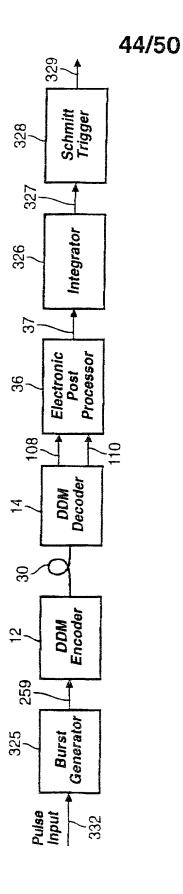


FIG. 4

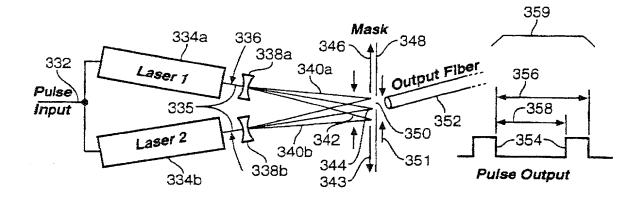


FIG. 45

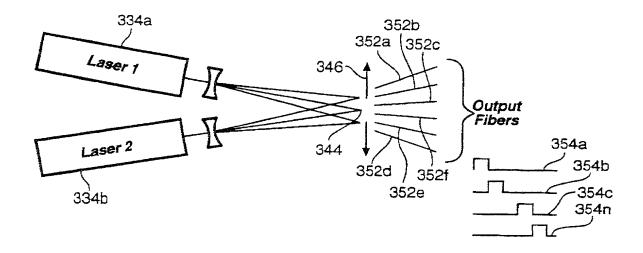


FIG. 46

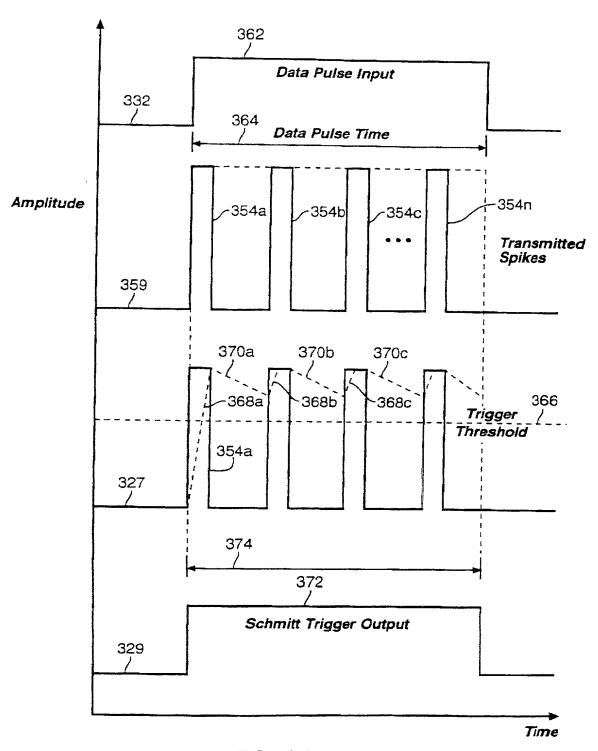


FIG. 47



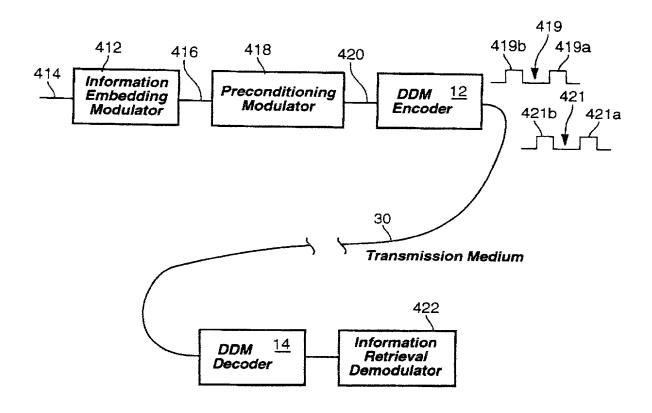


FIG. 48

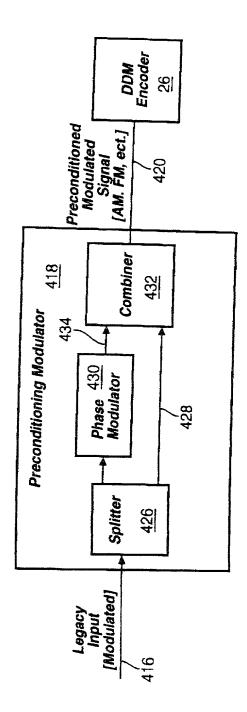


FIG. 49

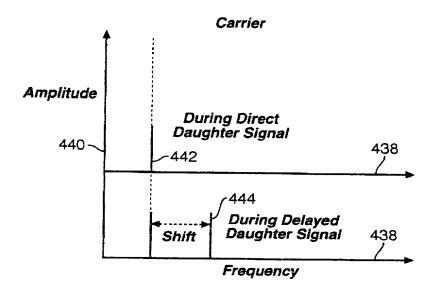


FIG. 50